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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/595,157

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Toshiaki Takenaka

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EXAMINER

GOFF II, JOHN L

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/595,157	Applicant(s) TAKENAKA ET AL.	
	Examiner John L. Goff	Art Unit 1791	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 November 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 November 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is in response to the amendment filed on 11/4/08.
2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Objections

3. Claims 1-14 are objected to because of the following informalities: In claim 1, line 6 delete “being is” and insert therein - - being - -. In claim 12, line 5 delete “being is” and insert therein - - being - -. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. Claims 1, 3, 5-9, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (Specification pages 1-4, 8, and 9) in view of Pommer (U.S. Patent 6,560,844).

The admitted prior art discloses a conventional method of manufacturing a multi-layer circuit board comprising providing a structure including a core circuit board having a circuit pattern thereon and a prepreg sheet having a through-hole filled with conductive paste sandwiched between a pair of metal foils further sandwiched between a pair of lamination plates and applying heat and pressure to form a laminated structure (Figures 6A-6D and Page 3, line 6 to Page 4, line 8). The admitted prior art does not specifically teach the lamination plates are selected to have a thermal expansion coefficient (TCE) equivalent to a TCE of the core circuit

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board. However, selecting lamination plates to have a TCE equivalent to a layer of the laminated structure was known as evidenced by the admitted prior art wherein a TCE equivalent to the metal foil is chosen to prevent wrinkling. Further, it was known in the art that each layer of the laminated structure, e.g. a structure including circuit board and prepreg layers as depicted in Figure 1, should have substantially similar considered equivalent TCE and that the lamination plates are selected to have a TCE the same as the TCE of the layers as shown by Pommer to prevent distortion of the layers (Figures 1 and 3 and Column 2, lines 3-5 and 44-49). It would have been obvious to one of ordinary skill in the art at the time the invention was made to practice the method as taught by the admitted prior art wherein all of the layers of the structure have equivalent TCE to prevent distortion of the layers as taught by Pommer thereby including selecting a lamination plate whose TCE is equivalent to the core circuit board.

Regarding claim 3 and 6, the admitted prior art teaches the core circuit board has four or more layers. The admitted prior art teaches the core circuit board and the prepreg sheet are alternately laminated so as to have two or more layers.

Regarding claims 7 and 8, the admitted prior art further teaches a buffer material considered formed of a material capable of accommodating difference in TCE between the lamination plate and a carrying plate disposed outside the structure which structure is placed on a heat press plate considered the carrying plate such that heat and pressure goes through the buffer material and the carrying plate. It would have been obvious to one of ordinary skill in the art at the time the invention was made to practice the method as taught by the admitted prior art wherein all of the layers in the lamination have equivalent TCE to prevent distortion of the layers

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as taught by Pommer thereby including selecting a carrying plate whose TCE is equivalent to the lamination plate.

Regarding claim 9, the admitted prior art teaches the prepreg sheet contains a base and a resin layer impregnated with the base to form a resin layer on both surfaces of the base.

Regarding claims 11 and 12, Pommer is considered to require measuring the TCE of all of the layers including the core circuit board otherwise selecting a lamination plate with an equivalent TCE would not be possible.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Pommer as applied to claims 1, 3, 5-9, 11, and 12 above, and further in view of Ikeguchi et al. (JP 57011026 and see also the abstract).

The admitted prior art and Pommer as applied above teach all of the limitations in claim 2 except for a specific teaching that the thickness of the resin layer formed on both sides of the base is at least 20 microns in total thickness. Ikeguchi disclose a prepreg excellent in workability comprising a base and a resin layer impregnated with the base to form a resin layer on both sides of the base having at least 20 microns in total thickness (See the abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the resin layers on both sides of the base as taught by the admitted prior art as modified by Pommer with a thickness at least 20 microns in total as shown by Ikeguchi to form a prepreg excellent in workability.

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6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Pommer as applied to claims 1, 3, 5-9, 11, and 12 above, and further in view of Shirasawa et al. (U.S. Patent 4,614,559).

The admitted prior art and Pommer as applied above teach all of the limitations in claim 4 except for a specific teaching that the core circuit board is not less than one time as thick as the prepreg sheet. Shirasawa directed to manufacturing a multi-layer circuit board comprising core circuit boards and prepreg sheets teach the layers are desirably as thin as possible to form a dimensionally stable board including specifically demonstrating the core circuit boards are not less than one time as thick as the prepreg sheets (Column 1, lines 33-35 and Tables 1 and 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use as the core circuit board and prepreg sheet in the admitted prior art as modified by Pommer layers as thin as possible including wherein the core circuit board is not less than one time as thick as the prepreg sheet as shown by Shirasawa to form a multi-layer circuit board that is thin and dimensionally stable.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Pommer as applied to claims 1, 3, 5-9, 11, and 12 above, and further in view of Del (U.S. Patent 4,180,608).

The admitted prior art and Pommer as applied above teach all of the limitations in claim 10 except for a specific teaching that the base is woven and the resin is B-staged. It is considered extremely well known in the art that a prepreg generally comprises a woven base and a B-staged resin as evidenced by Del (Column 4, lines 23-27). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the prepreg taught by the

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admitted prior art as modified by Pommer as was generally well known including a woven base and a B-staged resin as evidenced by Del only the expected results being achieved.

8. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Pommer as applied to claims 1, 3, 5-9, 11, and 12 above, and further in view of Levit (U.S. Patent Application Publication 2005/0230072).

The admitted prior art and Pommer as applied above teach all of the limitations in claims 11-14 except for a specific teaching that the TCE for each layer is measured by measuring the TCE at two positions or more in a range from room temperature to a heat pressing temperature by using a thermomechanical measurement apparatus and calculating an average value of the TCE from the two positions or more, it being noted Pommer is not limited to any particular technique for measuring the TCE for each layer. Levit is exemplary of measuring the TCE of a layer for use in a circuit board wherein determining the TCE for the layer includes measuring the TCE at two positions or more in range from room temperature to a heat pressing temperature by using a thermomechanical measurement apparatus and calculating an average value of the TCE from the two positions or more (Paragraphs 0011, 0030, and 0038). It would have been obvious to one of ordinary skill in the art at the time the invention was made to measure the TCE for each layer of the structure taught by the admitted prior art as modified by Pommer to determine that each layer has an equivalent TCE as required by Pommer wherein a known suitable technique for determining the TCE was disclosed by Levit.

Response to Arguments

9. Applicant's arguments filed 11/4/08 have been fully considered but they are not persuasive. The previous objections to the drawings and 35 USC 112 rejections have been overcome. The substitute specification has been entered.

Applicants argue, "In other words, although Pommer teaches that each layer and the alignment plate have a similar thermal expansion coefficient, Pommer still fails to disclose or suggest specifically that the thermal expansion coefficient of the core circuit board is similar to that of the pair of lamination sheets, as recited in claim 1."

The alignment plate taught by Pommer is considered a lamination plate. Further, Pommer is evidence that each layer, i.e. the metal foils, prepreg sheets, core circuit board, and lamination sheets, should all have substantially similar considered equivalent TCE to prevent distortion of the layers.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

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however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **John L. Goff** whose telephone number is **(571)272-1216**. The examiner can normally be reached on M-F (7:15 AM - 3:45 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on (571) 272-1226. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/John L. Goff/
Primary Examiner, Art Unit 1791